8751H/8753H

Single-Chip 8-Bit Microcontroller

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- Military Temperature Range
  - −55 to +125°C (T_C)
- 4K x 8 EPROM (8751); 8K x 8 EPROM (8753)
- 128 x 8 RAM
- 64K bytes Program Memory space
- 64K bytes Data Memory space
- Pin-compatible with entire 8051 Family
- Full-duplex programmable serial ports
- 32 I/O lines (four 8-bit ports)
- Supports Adaptive EPROM Programming
- EPROM Security Feature
- Two 16-bit Timer/Event counters

GENERAL DESCRIPTION

The 8751H and 8753H are members of a family of advanced single-chip microcontrollers. Both the 8751H, which has 4K bytes of EPROM, and the 8753H, which has 8K bytes of EPROM, are pin-compatible EPROM versions of the 8051AH and 8053AH, respectively. Thus, the 8751H/8753H are full-speed prototyping tools which provide effective single-chip solutions for controller applications that require code modification flexibility. Refer to the block diagram of the 8051 family.

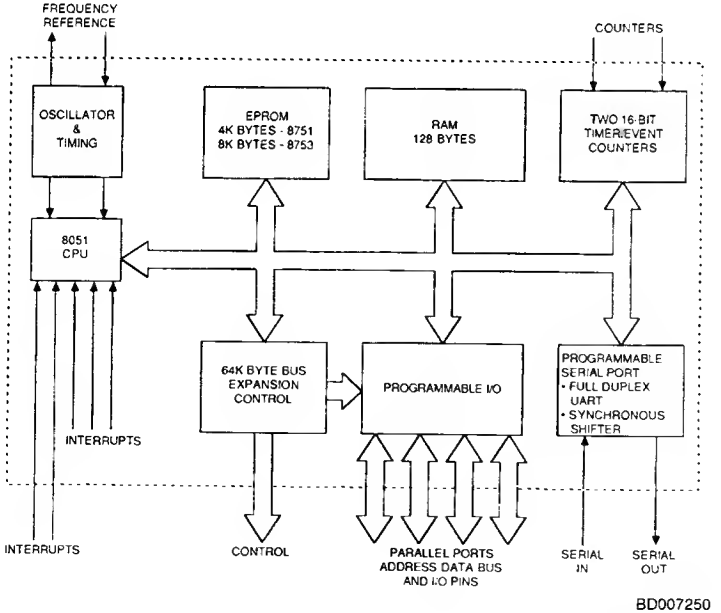
The 8751H/8753H devices feature: thirty-two I/O lines; two 16-bit timer/event counters; a Boolean processor, a 5-source, bi-level interrupt structure; a full-duplex serial channel; and on-chip oscillator and clock circuitry.

Program and Data Memory are located in independent addresses. The AMD family of microcontrollers can access up to 64K bytes of external Program Memory and up to 64K bytes of external Data Memory. The 8751H and the 8753H contain the lower 4K and 8K bytes of Program Memory, respectively, on-chip. Both parts have 128 bytes of on-chip read/write data memory.

The AMD 8051 Microcontroller Family is specifically suited for control applications. A variety of fast addressing modes, which access the internal RAM, facilitates byte processing and numerical operations on small data structures. Included in the instruction set is a menu of 8-bit arithmetic instructions, including 4-cycle multiply and divide instructions.

Extensive on-chip support enables direct bit manipulation and testing of 1-bit variables as separate data types. Thus, the device is also suited for control and logic systems that require Boolean processing.

BLOCK DIAGRAM



BD007250

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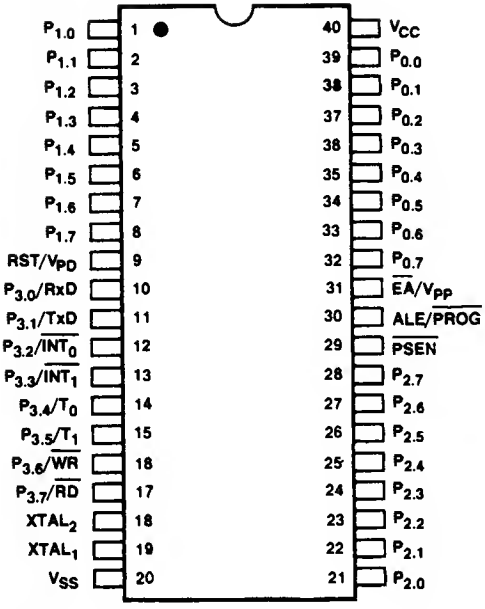
CONNECTION DIAGRAMS
Top View



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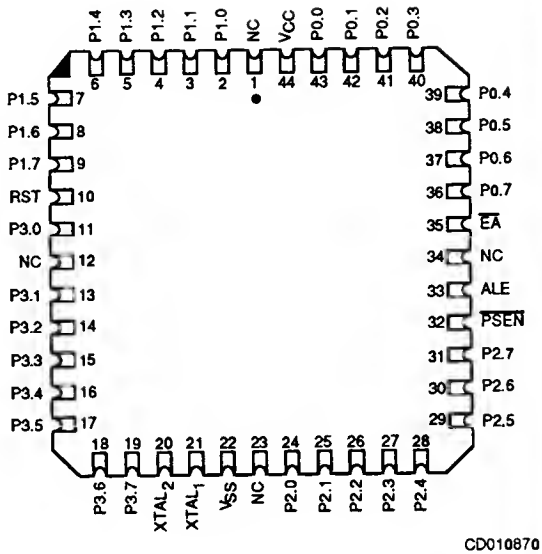

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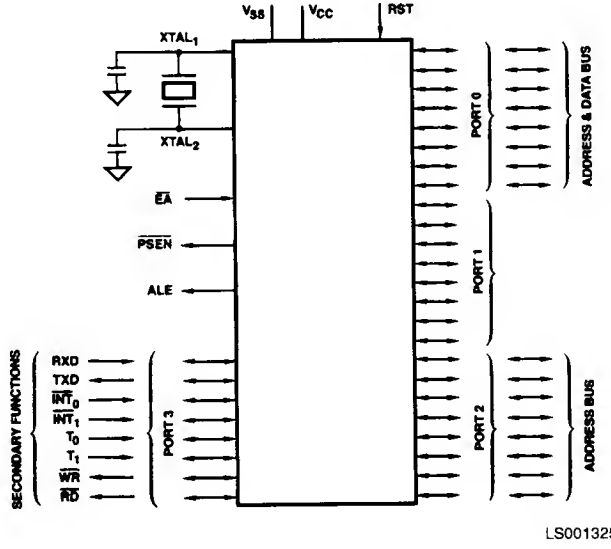
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

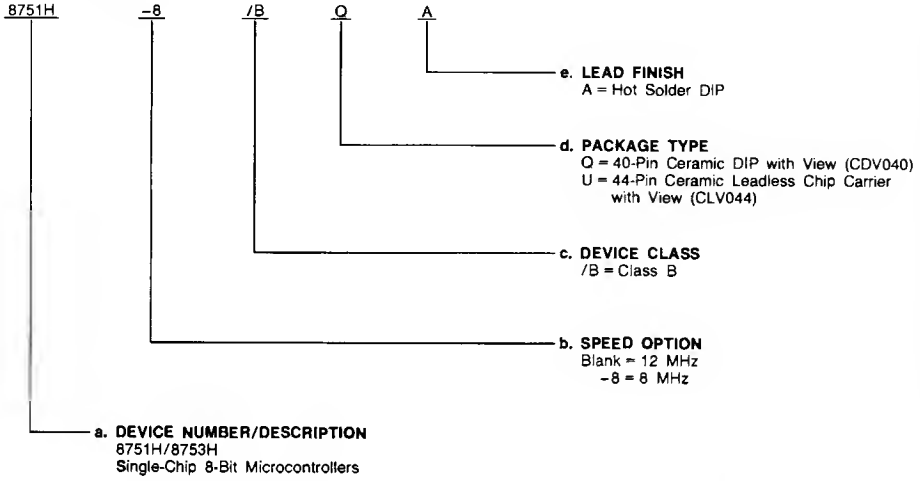


LS001325

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8751H	/BQA, /BUA
8751H-8	
8753H	
8753H-8	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Other Pin to V_{SS}
(Except V_{PP}) ..... −0.5 to +7.0 V
Voltage from V_{PP} to V_{SS} ..... −0.5 to +21.5 V
Power Dissipation ..... 2 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V
Ground (V_{SS}) ..... 0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL} †	Input LOW Voltage		−0.5	0.7	V
V_{IL1} †	Input LOW Voltage to $\overline{EA}$		0	0.7	V
V_{IH} †	Input HIGH Voltage (Except $XTAL_2$, RST)		2.2	V_{CC} + 0.5	V
V_{IH1} †	Input HIGH Voltage to $XTAL_2$, RST	$XTAL_1$ = V_{SS}	2.5	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage (Ports 1, 2, 3) (Note 1)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output LOW Voltage (Port 0, ALE, $\overline{PSEN}$) (Note 1)	I_{OL} = 3.2 mA		0.60	V
		I_{OL} = 2.4 mA		0.45	
V_{OH}	Output HIGH Voltage (Ports 1, 2, 3)	I_{OH} = −60 μA	2.4		V
V_{OH1}	Output HIGH Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)	I_{OH} = −300 μA	2.4		V
I_{IL}	Logical 0 Input Current P1, P2, P3	V_{IN} = 0.45 V		−500	μA
I_{IL1}	Logical 0 Input Current to $\overline{EA}$/V_{PP}	V_{IN} = 0.45 V		−15	mA
I_{IL2}	Logical 0 Input Current to $XTAL_2$	$XTAL_1$ = V_{SS}, V_{IN} = 0.45 V		−4.5	mA
I_{LI}	Input Leakage Current to Port 0	0.45 < V_{IN} < V_{CC}		±100	μA
I_{IH}	Logical Input Current to $\overline{EA}$/V_{PP}	V_{IN} = 2.4 V		500	μA
I_{IH1}	Input Current to RST/V_{PD} to Activate Reset	V_{IN} < (V_{CC} − 1.5 V)		500	μA
I_{CC}	Power Supply Current (Note 3)	All Outputs Disconnected, $\overline{EA}$ = V_{CC}		275	mA
C_{IO} ††	Capacitance of I/O Buffers	f_C = 1 MHz, T_A = 25°C		30*	pF
I_{PD}	Power-Down Current (Note 2)	T_A = 25°C, V_{PD} = 5.0 V, V_{CC} = 0 V		10	mA

Notes: 1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Power-Down I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = V_{CC} = 0; $XTAL_2$ = N.C.; RST = V_{PD} = 5.0 V.
3. I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 5 V, V_{IH} = V_{CC} − 5 V; $XTAL_2$ = N.C.; $\overline{EA}$ = RST = V_{CC}.

† Group A, Subgroups 7 and 8 only are tested.
†† Not included in Group A tests.
* Not tested; guaranteed by design.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)
(Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

External Program Memory Characteristics

Parameter Symbol	Parameter Description	12-MHz Osc.		8-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$1/t_{CLCL}$	Oscillator Frequency	3.5	12	3.5	8	3.5	12	MHz
t_{LHLL}	ALE Pulse Width	112		195		$2t_{CLCL}-55$		ns
t_{AVLL}	Address Setup to ALE	28		70		$t_{CLCL}-55$		ns
t_{LLAX}	Address Hold After ALE	33		75		$t_{CLCL}-50$		ns
t_{LLIV}	ALE to Valid Instr In		168		335		$4t_{CLCL}-165$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	43		85		$t_{CLCL}-40$		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	175		300		$3t_{CLCL}-75$		ns
t_{PLIV}	$\overline{PSEN}$ to Valid Instr In		85		210		$3t_{CLCL}-165$	ns
t_{PXIX}	Input Instr Hold After $\overline{PSEN}$	0		0		0		ns
t_{PXIZ}	Input Instr Float After $\overline{PSEN}$		48		90		$t_{CLCL}-35$	ns
t_{PXAV}	Address Valid After $\overline{PSEN}$	58		100		$t_{CLCL}-25$		ns
t_{AVIV}	Address to Valid Instr In		252		460		$5t_{CLCL}-165$	ns
t_{PLAZ}	Addr Float After $\overline{PSEN}$		20		20		20	ns

External Data Memory Characteristics

Parameter Symbol	Parameter Description	12-MHz Osc.		8-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RLRH}	$\overline{RD}$ Pulse Width	400		650		$6t_{CLCL}-100$		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		650		$6t_{CLCL}-100$		ns
t_{LLAX}	Address Hold After ALE			75		$t_{CLCL}-50$		ns
t_{RLDV}	$\overline{RD}$ to Valid Data In		232		440		$5t_{CLCL}-185$	ns
t_{RHDX}	Data Hold After $\overline{RD}$			0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		82		165		$2t_{CLCL}-85$	ns
t_{LLDV}	ALE to Valid Data In		496		830		$8t_{CLCL}-170$	ns
t_{AVDV}	Address to Valid Data In		565		940		$9t_{CLCL}-185$	ns
t_{LLWL}	ALE to $\overline{RD}$ or $\overline{WR}$	185	315	310	440	$3t_{CLCL}-65$	$3t_{CLCL}+65$	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$	188		355		$4t_{CLCL}-145$		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	0		40		$t_{CLCL}-85$		ns
t_{QVWH}	Data Setup Before $\overline{WR}$	508		800		$7t_{CLCL}-75$		ns
t_{WHQX}	Data Hold After $\overline{WR}$	18		60		$t_{CLCL}-65$		ns
t_{RLAZ}	Address Float After $\overline{RD}$		20		20		20	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	18	148	60	190	$t_{CLCL}-65$	$t_{CLCL}+65$	ns

External Clock Drive*

Parameter Symbol	Parameter Description	Min.	Max.	Unit
$1/t_{CLCL}$	Oscillator Frequency	1.2	12	MHz
t_{CHCX}	HIGH Time	20		ns
t_{CLCX}	LOW Time	20		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

*Not tested; these specs are controlled by the Teradyne J941, J983 tester.

SWITCHING CHARACTERISTICS (Cont'd.)
Serial Port Timing — Shift Register Mode (C_L = 8 pF)

Parameter Symbol	Parameter Description	12-MHz Osc.		8-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		1.0		$12t_{CLCL}$		μs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		1117		$10t_{CLCL}-133$		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	49		133		$2t_{CLCL}-117$		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		1117		$10t_{CLCL}-133$	ns

EPROM Programming and Verification Characteristics
(T_A = +21 to +27°C, V_{CC} = +5 V ±10%, V_{SS} = 0 V)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
V_{PP}	Programming Supply Voltage	20.5	21.5	V
I_{PP}	Programming Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	4	6	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	$P_{2.7}$ ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$	10		μs
t_{GHSL}	V_{PP} Hold after $\overline{PROG}$	10		μs
t_{GLGH}	$\overline{PROG}$ Width	45	55	ms
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	

*Not tested; guaranteed by design.